A Statistical Approach to 0201 Component Package Utilization

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ABSTRACT

An experiment was designed to investigate the process characteristics associated with reflow soldering 0201 component packages, in general and, specifically, determine the specification limits for 0201 placement accuracy. Low defect rates and component placement Cp, Cpk above 2.0 were attained. These counterintuitive results for components this small are attributed to two primary factors: 1. the relative magnitude of the reflow wetting forces generated that tend to move the component compared to those that act to hold the component in place and, 2., the high accuracy and repeatability of the placement equipment available today. The time/temperature reflow ramp rate emerged as the process parameter with the narrowest process window. This result is attributed to the tendency of the small volumes of solder paste printed for 0201's to oxidize more quickly when heated than those printed for larger components. This oxidation interferes with the ability of the Sn/Pb solder spheres to properly melt when the alloy's liquidus temperature is reached. An oven profile that results in a straight, relatively rapid temperature ramp rate of close to 2.0 deg. C per sec. was found to yield excellent reflow soldering characteristics.

INTRODUCTION

The general subject of this paper is electronic product assembly. More specifically, the production of the circuit board subassembly commonly found in most electronic products, and the use of the emerging 0201 component package in those subassemblies.

This paper was initially undertaken to develop a model that could be used to assist in determining the true cost of designing 0201 packages into circuit board assemblies. The model was to use empirical data derived from an experiment designed to establish the assembly process "cost of use." Another statement that was made in the original paper objective abstract: *If 0201's must be used for an application, the model helps predict their incremental cost impact*, implied that 0201's should be used only if you had to, and there would be a negative cost impact if they were. The results of the work done since that initial objective abstract demonstrate that this is not necessarily so. This paper documents the work that was done to support this conclusion.

Confusion in terminology has developed over the years concerning the use of the words *manufacturing* and *assembly*. Years ago an attempt was made by some to draw a distinction between the two by suggesting the term *manufacturing* in electronic or electromechanical products should be reserved to describe the process of individual part or component production (e.g., gears, threaded fasteners, monolithic chip capacitors, bare circuit boards, etc.). The term *assembly* could then be used to describe the process of putting individual manufactured parts together. Hence, the phrase "Design for Manufacturing and Assembly" or, DFMA, referred both to optimizing designs for lowest cost part fabrication (manufacturing) and combining those parts into products (assembly). Based on the observed practice in the literature over the last several years of freely using these terms interchangeably, it can be safely stated that the battle for this literary convention has been an unabashed failure. In any event, this paper will adhere to the well-intentioned convention.

The 0201 component package is problematic for a number of reasons, not the least of which is that you can't see one with the unaided eye. Some younger colleagues may make statements to the contrary, but these claims are tantamount to claiming Freddie the Flea just jumped through a hoop – you saw him, didn't you? Uh, of course!

So, what are the implications of using this pepper-like package in a circuit board assembly operation? The position this research started from was that an attempt should be made to quantify the effects and not rely on conjecture, hyperbole, and anecdotal reports. The path to these data was accompanied by some counterintuitive experiences. These surprises underscored the importance of using empirical data to make decisions that can affect the ultimate cost of the assembled product.

This anticipated cost is clearly an important element needed to conduct the appropriate cost / benefit and risk analyses necessary to judge whether 0201's should be used for specific product applications.

First presented at SMTA International, Chicago, IL., September 2002.

This conclusion concerning the non-negative assembly cost impact is based on the surprising robustness of the process that was developed for the study. This unanticipated wide process window especially manifested itself in certain aspects the paste printing and component placement process steps. Conversely, the results obtained demonstrated an acute sensitivity to process parameters such as reflow time-temperature ramp rate. These observations, while commented on here, will be the subject of more detailed study in subsequent research.

One summary conclusion that the experimental data strongly supports is that 0201's can provide higher component density board designs (smaller products), improved high clock speed performance (shorter electrical distances), and reduced product weight without having to pay a price premium for reduced assembly yields. The conditions leading to the attainment of this result, however, are not trivial. They require the right combination of equipment, board design, assembly process development and assembly process control.

It is this superposition of many factors, including considering the specific application, in many possible combinations that make the development of a spreadsheet cost model unrealistic. What the paper does do is provide general process goals and considerations for successful 0201 implementation based on a statistical treatment of the experimental data. Some of these are:

- The process used printed paste in an "off-contact" fashion resulting in a Hershey's Kiss™ or mound geometry, rather then the traditional brick.
- The paste was had a no-clean chemistry and used standard 63/37 Type 3 spheres.
- Very high Cp and Cpk placement process indices can be obtained.
- Reflow ramp rates should be rapid to avoid paste oxidation.

THE 0201 PACKAGE

Physical Characteristics

Figure 1 contains the family of passive, chip component packages placed on a Roosevelt dime. Figure 2 provides the nominal dimensions for the newest family member, the 0201 package. Figure 3 adds this newest member to the passive, chip component family photo.

Weighing about a 1000, 0201's resulted in a weight of one component to be about 0.227 mg, or somewhere between a grain of salt and a grain of pepper.

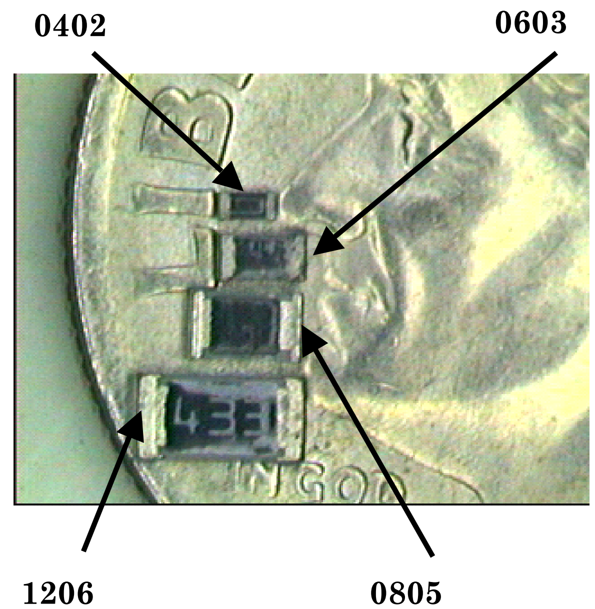
0201 PROCESS CONDITIONS

The Test Board

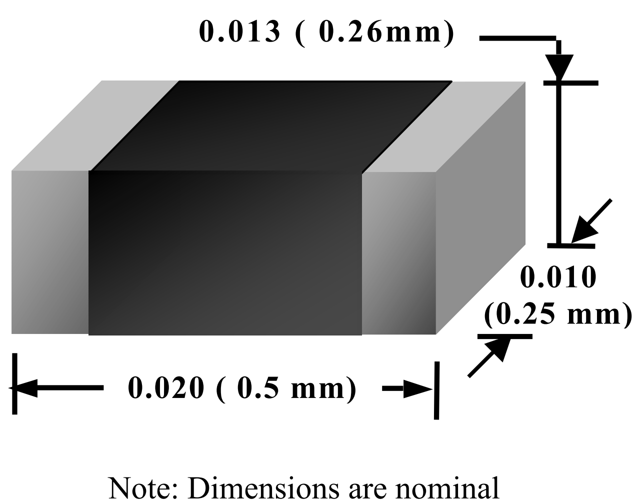
An existing placement machine demo circuit board panel was used for the experiment. The panel had 200, 0201 pad sets clustered in 2, 10 x 10 arrays. The pads were finished using a standard hot air solder level (HASL) process.

Paste Printing

The stencil designed for the study was 0.005 in. thick stainless, laser cut to full pad dimensions and photo-polished. Printing was done "off-contact" using a standard Type 3 sphere diameter, 63/37 solder paste with a no-clean flux chemistry. The "off-contact" decision was made because of the desire to print a larger paste volume per pad than a contact print process would afford.

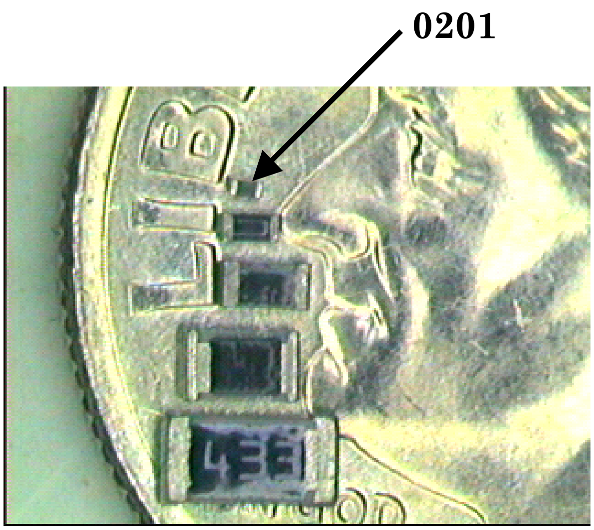


Passive Chip Component Family
Figure 1



The 0201 (0603) Package
Figure 2

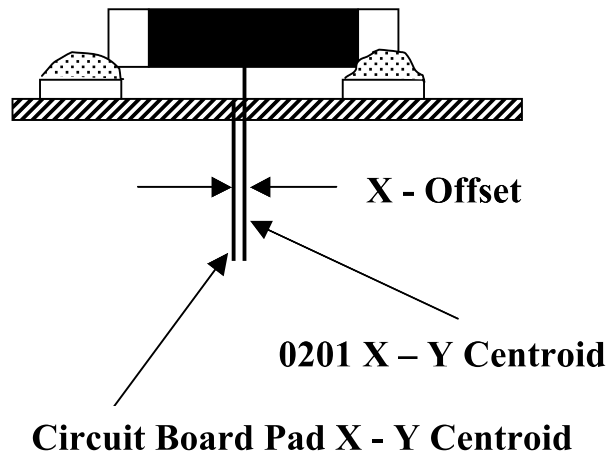
post-reflow solder defects as a function of these "dialed-in" offsets.



Package	L	W	H
0201 (0603)	.021	.011	.011
0402 (1005)	.039	.020	.013
0603	.063	.033	.017
0805	.079	.050	.020
1206	.121	.061	.021

Dimensions are in inches

Passive Chip Component Family
With the 0201 Package Added
Figure 3



0201 Placement X - Offset
Figure 4

Another product of the "off-contact" technique was a pyramid/conical-shaped print. The contribution (if any) this had on the high Cp / Cpk index values achieved requires additional study. One thing fairly certain is that this condition did contribute to the relatively large number of acceptable solder joints achieved during worst-case x-offset (long axis) placement condition. This placement condition created a nominal .0015 gap between one end of the 0201 component and its printed pad prior to reflow! A theory explaining this highly unanticipated result is offered in the paragraph labeled "Discussion of Results."

Component Placement
The 0201 components were presented to the placement machine on tape and reel. Parts were accessed and placed at speed with normal machine placement pressure. A series of x-axis offsets to the nominal pad centroid locations were introduced via machine programming to establish specification control limits for 0201 component placement (see Figure 4). This spec. control limit was determined by

Solder Reflow
An in-line, 4T - 4B forced air convection reflow oven was used to bring the solder paste to its 183 deg. C liquidus point. Early trial runs were not successful in melting the paste even though a circuit board thermal profiler indicated board temperatures in the 220 deg C range. During these runs the temperature rise rates were between 0.9 and 1.3 deg C per sec. It was postulated that as the relatively small amount of flux associated with the small amount of solder paste printed on the 0201 pads was progressively heated and thinned, it quickly spread leaving the solder spheres exposed to the heated air in the oven. This accelerated the solder's oxidation that, in turn, interfered with the sphere's ability to melt, coalesce and wet to the component end terminations and circuit board pads. The hypothesis was confirmed when straight ramp rates of above 1.6 deg C. to a peak temperature of about 216 deg. C resulted in excellent solder wetting. It was concluded that a rather narrow ramp rate window of between 1.6 and 2.0 deg C per sec. was required. This narrow specification tolerance could probably be increased with the use of an inert oven gas such as Nitrogen. However, with the low variation from target ramp rates provided by tight microprocessor control, the use of Nitrogen with most ovens is not considered necessary.

EXPERIMENTAL PROCEDURE

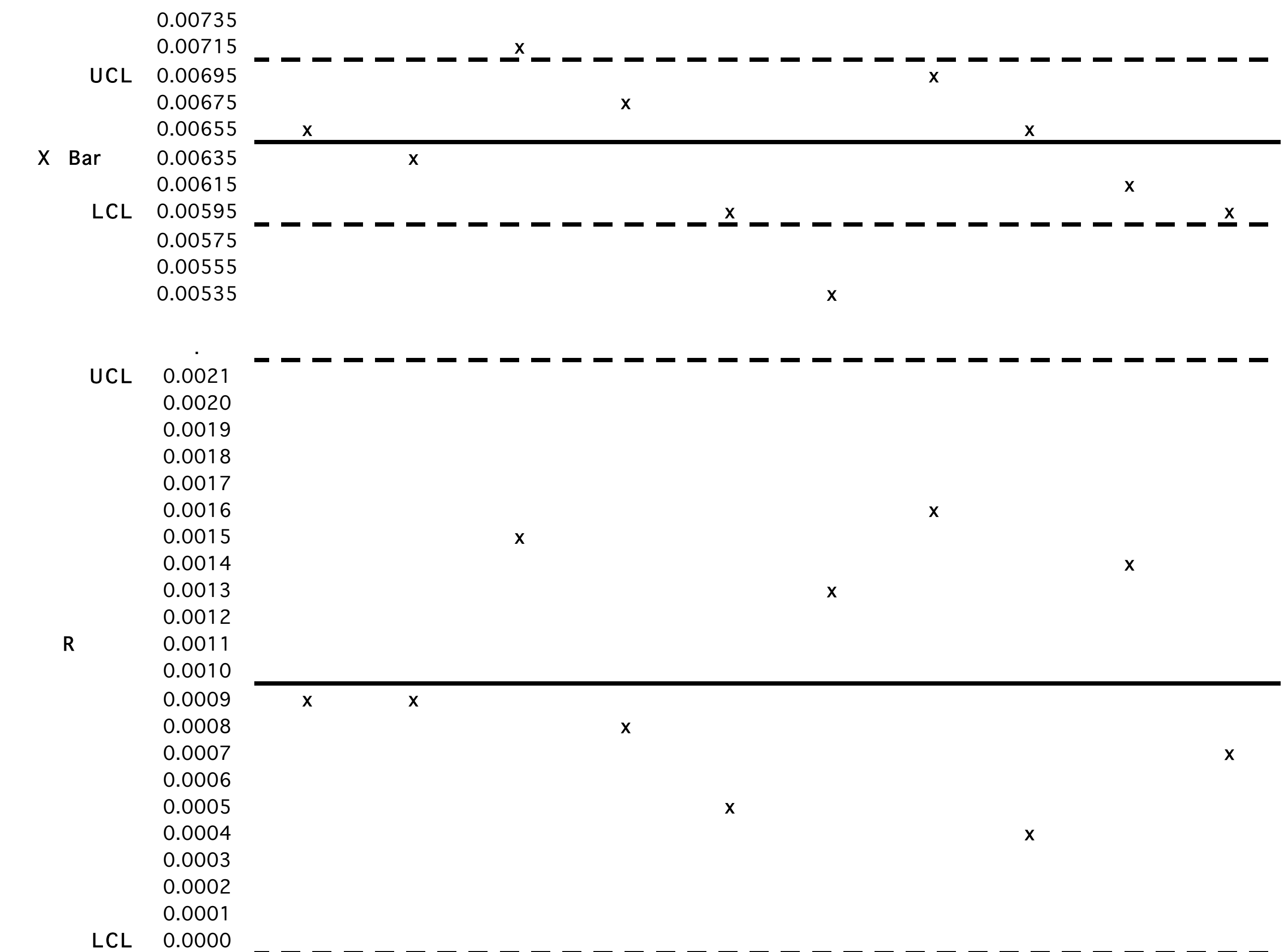
A 0.001 in. placement x-offset was machine programmed to establish the variance around this target offset value. Figure 5 presents the X bar and R graphs for this run. The data is fairly well behaved. Two points lie outside control limits. These data are attributed to measurement error.

Run With .001 in. X-Placement Offset (Nominal Placement Measurement = .0065 in.)

Figure 5

		Subgroups 1	2	3	4	5	6	7	8	9	10
	1	0.0072	0.0062	0.0066	0.0064	0.0063	0.0053	0.0074	0.0067	0.0058	0.0059
Sample Measure.	2	0.0066	0.0070	0.0072	0.0067	0.0062	0.0065	0.0082	0.0064	0.0061	0.0061
	3	0.0063	0.0061	0.0075	0.0067	0.0058	0.0052	0.0069	0.0064	0.0066	0.0062
	4	0.0072	0.0063	0.0069	0.0069	0.0058	0.0054	0.0066	0.0067	0.0055	0.0056
	5	0.0063	0.0067	0.0081	0.0072	0.0058	0.0052	0.0066	0.0068	0.0069	0.0063
Sum		0.0336	0.0323	0.0363	0.0339	0.0299	0.0276	0.0357	0.0330	0.0309	0.0301
X Bar		0.00672	0.00646	0.00726	0.00678	0.00598	0.00552	0.00714	0.0066	0.00618	0.00602
R		0.0009	0.0009	0.0015	0.0008	0.0005	0.0013	0.0016	0.0004	0.0014	0.0007

X Double Bar	0.006466
R Bar	0.001
UCL X Bar	0.007043
LCL X Bar	0.005889
UCL R	0.002114
LCL R	0



Sample Standard Deviation 0.00043 With a +/- 0.003 specification limit around a target value of 0.0065, Cp= 2.33 Cpk= 2.35

(Note: See "Results" section for explanation of specification limits)

With this condition, the data were judged to be normally distributed. The average of measured placement location subgroup averages (X double bar) was 0.00647. This was exactly the programmed target value of 0.0065. The average difference between the largest and smallest measurement in each subgroup was 0.001 in.

Additional boards were built with varying nominal placement x-offsets of up to 0.007 inches to establish 0201 placement specification limits. After reflowing each case, the 200, 0201 components per board were inspected for solder defects and process indicators. Inspection was done in accordance with the requirements of J-STD-001 (using the acceptability requirements of ANSI/IPC-A-610 Rev. B). The following code was developed to document the post-reflow results:

No entry = acceptable solder joint

1 = some component to pad misalignment - both end terminations are at least 75% on their respective pads with acceptable solder fillets. (process indicator)

2 = electrical contact with acceptable solder fillets - either termination is less than 75% on its respective pad (judged “defective” for this experiment)

3 = No electrical contact between an end termination and pad or an unacceptable solder joint (fatal defect)

S = Defect due to something other than the placement offset. (e.g., no paste on pad)

The results were recorded on a defect map. Figure 6 is an example of a defect map for the 0.004 in. offset case.

Figure 6 – Defect Map for 0.004 Offset Case (Board #1000)

			1	1		2			
				1	1				
			1					1	
	1		1				1	1	
		1	1	1				1	1
1			1	1					1
1			1	1		1			
						S			
									1
		1				1	1		

				1			1	1	
		1	2			1	1	1	1
						1	1		
	1			1	1				
					1	1			1
2						1	1	2	
1	1	1	1		1		1		
		1	2	1	1		1	1	
							1		2
	1								2

Each cell on the map represents an 0201 component location on the test board. The code is used to record the post-solder results.

RESULTS

Table 1 provides the results of the experiment.

x-offset (inches)	# of 0201 Components Processed	Indicator/Defect Type 1	2	3	Total PPM Defect Rates
0.000	200	0	0	0	0
0.001	400	0	0	0	0
0.003	1000	7	0	0	0
0.004	400	76	14	0	35,000
0.007	200	31	11	21	165,000

Solder Results as a Function of x-offset
Table 1

The results are conservation since it is debatable if a Type 2 condition should be counted as a rejectable defect. For this experiment, large populations of 0201 were not processed, therefore, the conservation judgement on the Type 2 condition is appropriate. In any event, the 0.003 offset case emerges as one end of a conservative placement specification limit. The total specification tolerance, therefore, is 0.006 inches.

DISCUSSION OF RESULTS

Figure 7 provides the X bar and R charts for a typical set of 0.003 offset data. The process indices, Cp and Cpk are both calculated as 1.99. Based of these data the process is judged to be both in control and capable. The large process index values suggest that with this tight placement distribution and relatively large process tolerance, the process would need to go significantly out of control to require investing resources to correct. (i.e., a moderately out of control process would probably not result in solder defects caused by placement inaccuracies). Or, said another way, the process window is wide enough to tolerate a significant amount of process variation, even if the variation is not in statistical control.

The most surprising result occurred when the nominal placement offset was set at 0.007. This literally put a nominal gap of 0.0015 inches between one end of the 0201 and the pad. (see Figure 8). A visual inspection prior to reflow clearly showed this gap at about 95% of the 0201 sites (or, about 190 of the 200 locations). Figure 9 is the defect map for this condition. Even though 32 of the components were judged rejectable (Type 2 and 3 defects), a startling 168 were deemed acceptable!

Run With .003 X-Placement Offset (Nominal Placement Target= .0075)
Figure 7

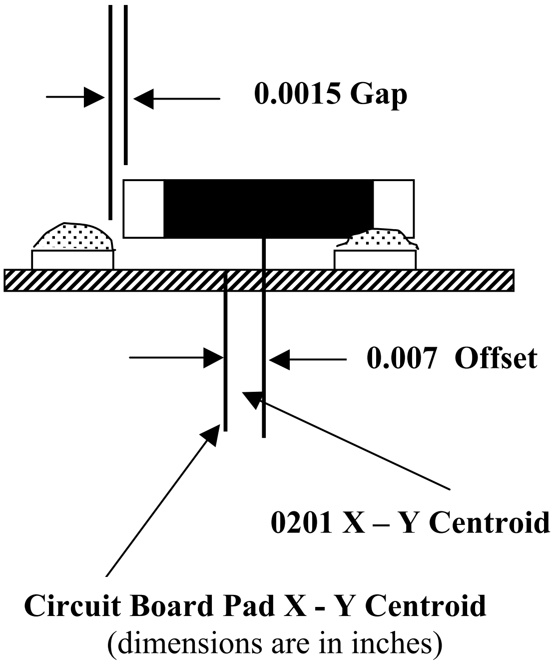
		Subgroups 1	2	3	4	5	6	7	8	9	10
Sample Measure.	1	0.0074	0.0071	0.0076	0.0072	0.0076	0.0074	0.0076	0.0077	0.0072	0.0076
	2	0.0082	0.0066	0.0081	0.0071	0.0070	0.0072	0.0069	0.0071	0.0072	0.0079
	3	0.0074	0.0083	0.0068	0.0079	0.0076	0.0078	0.0077	0.0082	0.0072	0.0090
	4	0.0070	0.0081	0.0075	0.0076	0.0080	0.0068	0.0070	0.0082	0.0069	0.0070
	5	0.0079	0.0071	0.0075	0.0081	0.0078	0.0078	0.0077	0.0068	0.0069	0.0078
Sum		0.0379	0.0372	0.0375	0.0379	0.0380	0.0370	0.0369	0.0380	0.0354	0.0393
X Bar		0.00758	0.00744	0.00750	0.00758	0.00760	0.00740	0.00738	0.00760	0.00708	0.00786
R		0.0012	0.0017	0.0013	0.0010	0.0010	0.0010	0.0008	0.0014	0.0003	0.002

X Double Bar	0.007502
R Bar	0.00117
UCL X Bar	0.008177
LCL X Bar	0.006827
UCL R	0.002473
LCL R	0

		1	2	3	4	5	6	7	8	9	10
UCL	0.00805										
	0.00795										
	0.00785										x
	0.00775										
	0.00765										
X Bar	0.00755	x			x	x			x		
	0.00745			x							
	0.00735		x				x	x			
	0.00725										
	0.00715										
	0.00705									x	
	0.00695										
	0.00685										
LCL	0.00680										

		1	2	3	4	5	6	7	8	9	10
UCL	0.0021										
	0.0020										x
	0.0019										
	0.0018										
	0.0017		x								
	0.0016										
	0.0015										
	0.0014								x		
	0.0013			x							
	0.0012	x									
R	0.0011										
	0.0010				x	x	x				
	0.0009										
	0.0008							x			
	0.0007										
	0.0006										
	0.0005										
	0.0004										
	0.0003									x	
	0.0002										
	0.0001										
LCL	0.0000										

Sample Standard Dev 0.000503 With a +/- 0.003 specification limit around a target value of 0.0075, Cp= 1.99 Cpk= 1.99



0.007 X - Offset Condition
Figure 8

1	1		1			1	1	1	
			1	2			1	3	
2					3				
1		3	1	1	1	1			1
1				1		1			3
	3					3	1		
	3				1	1			
3			1		2		2		3
	3				3				
2	2	1		1			3		

				1		3			
			1				3	3	
	2						3		
	2	3			1				3
1					1				
		1			1		3		
					3				
2									
3	2	S	1					2	

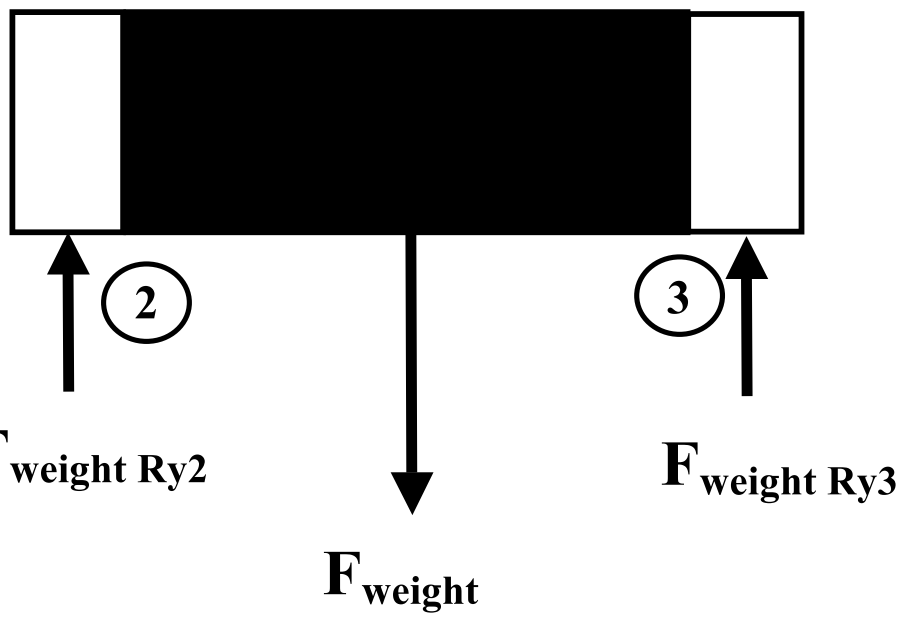
Figure 9 – Defect Map for 0.007 Offset Case
(Board #1100)

What mechanism caused components clearly separated from one of their solder pads before entering the oven, to be soldered to that pad upon exiting? The most plausible theory seems to have to do with the cantilevered condition of the 0201 existing prior to reflow and the relative forces present during reflow oven (see Figure 8). The component will move if subjected to unbalanced force (see figures 10 and 11). An unbalanced force can occur as solder wets up the end terminations of the component. If the difference in the x-component of these oblique wetting forces (Xwet & Xwet'), generates a moment at a point (say, Point 4 in Figure 11) that is greater than the opposing moments created by the component weight and wetting forces under the component, the component will tombstone. This moment is directly proportional to how far up the component this unbalanced force is acting and how much of the termination the solder is wetting to. The 0201 is very thin. It has been placed in this offset condition so the right end of the termination is not in full contact with the paste and some of the solder is in contact with the unmetalized body of the component (see Figure 8). Therefore, the difference in opposing moments is relatively small. In addition, the contact area between the solder and bottom of the termination that is in solder is relatively large. This tends to oppose any moment tending to lift the component.

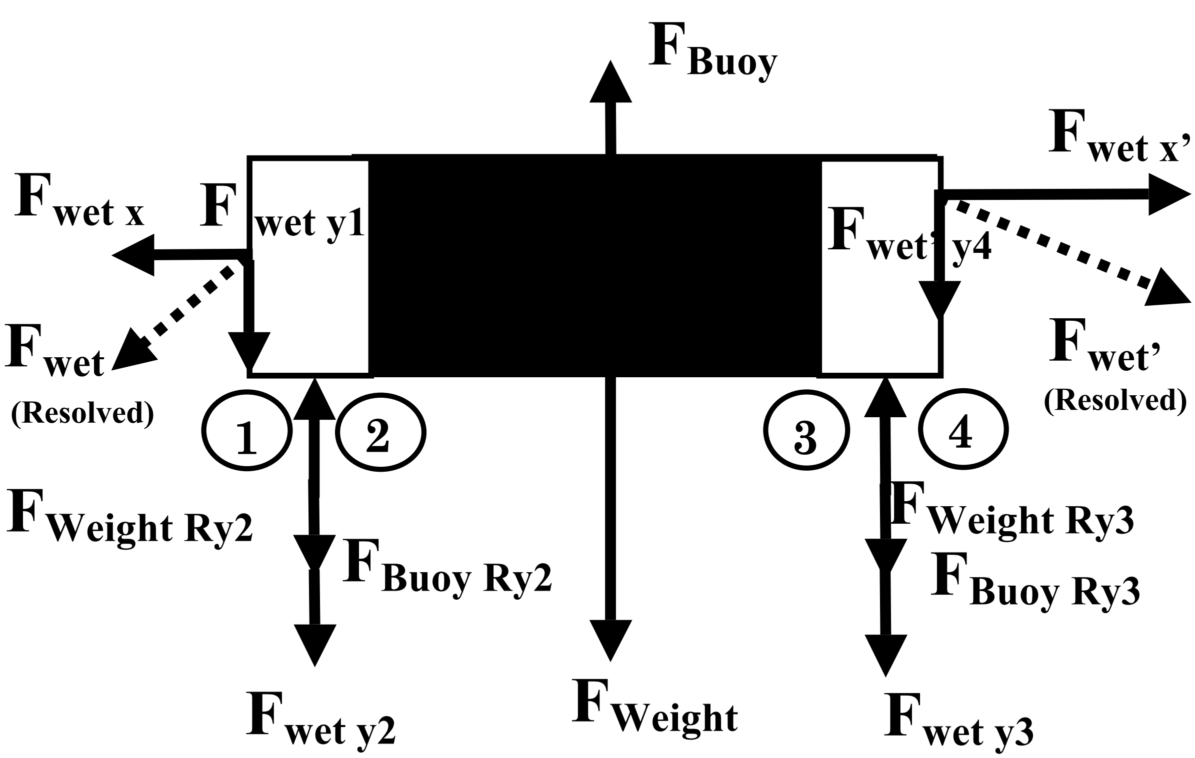
But how does the component end bridge the gap that is created by the 0.007 in. offset? As the solder melts the buoyant forces generated by the now liquid solder cause the cantilevered component to float up. The metalized termination immersed in the solder attempts to center itself on its pad. As it does, the component shifts in the x direction and closes the gap and, like an unbalanced seesaw, the unsupported end tips down and slides slightly permitting it to contact the liquid solder on the other pad. Upon contact, the wetting force pulls the component onto the, heretofore, unoccupied pad.

CONCLUSION

The experiment demonstrated that a highly capable, robust process can be developed for the 0201 component package. Therefore, with proper process development and control, the circuit board design density advantages afforded by using 0201 components can be realized without having to pay a premium for increased assembly cost.



Force Balance Prior to Solder Melt
Figure 10



Some of the Forces Present During Solder Melt
Figure 11

First presented at SMTA International, Chicago, IL., September 2002.